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EXAMINER	
HENN, TIMOTHY J	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 09/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/497,154	MONOI, MAKOTO	
	Examiner	Art Unit	
	Timothy J. Henn	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,5-20,22,23 and 25-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,5-20,22,23 and 25-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 14 July 2005 has been entered.

Response to Arguments

2. Applicant's arguments, see amendment, filed 14 July 2005, with respect to the rejection(s)of the claim(s) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Nakashiba (US 5,442,396).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Nakashiba (US 5,442,396).

[claim 7]

Regarding claim 7, Nakashiba discloses a solid image pickup apparatus comprising: a pixel string in which a plurality of photoelectric converting sections corresponding to pixels are arranged in one string (Figure 6, Items 21); a CCD register, adjacently arranged to the pixel string, for successively transferring in a predetermined direction, signal charges photoelectrically converted in the respective photoelectric converting sections (Figure 6, Items 23); a wiring layer formed above the CCD register and its periphery (Figures 7A - 7D, Items 28a and 28c) via an insulating layer (Figures 7A - 7D, Item 25); a shift electrode which is formed between the pixel string and the CCD register and which transfers, to the CCD register, the signal charges photoelectrically converted in the respective photoelectric converting sections in the pixel string (Figures 6, 7B and 7D, Item 26b; c. 9, l. 66 - c. 10, l. 68); a shift electrode wiring layer for applying a voltage for transferring electric charge to the shift electrode (Figures 7A - 7D, Items 28b and 28d) and a contact which has a longest length along a direction crossing substantially at right angles to an electric charge transfer direction under said shift electrode and which connects the shift electrode to the shift electrode wiring layer (Figures 6, 7B and 7D, contacts 27).

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 2, 3, 5, 6, 8-20 and 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakashiba (US 5,442,396) in view of Tanaka et al. (US 5,506,429).

[claim 2]

Regarding claim 2, Nakashiba discloses a solid image pickup apparatus comprising: a pixel string in which a plurality of photoelectric converting sections corresponding to pixels are arranged in one string (Figure 6, Items 21); a CCD register, adjacently arranged to the pixel string, for successively transferring in a predetermined direction, signal charges photoelectrically converted in the respective photoelectric converting sections (Figure 6, Items 23); a transfer electrode for supplying a voltage for transferring to the CCD register (Figures 7A and 7C, Items 26a); n (n is an integer of two or more) pieces of wiring layers formed in lamellar shape above the transfer electrode and its periphery (Figures 7A - 7D, Items 28a and 28c) via an insulating layer (Figures 7A - 7D, Item 25); and a contact having a longest length along an electric charge transfer direction (i.e. left to right along sheet 5 of the drawings, Figure 6) of the CCD register to at least one location between the transfer electrode and the wiring layer (Figures 6 and 7A - 7D, contacts 27). However, Nakashiba does not disclose a contact between two wiring layers adjacent to each other via the insulating layer.

Tanaka et al. discloses a "double-layered transfer gate" structure (Column 5, Lines 11-25) which prevents the occurrence of pulse delay and rounding of

pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka with the transfer electrode of the Nakashiba to prevent the occurrence of pulse delay and rounding of pulse wave-forms when driving the solid state image pickup apparatus. When an additional wiring layer is added to the structure of the Nakashiba, as taught by Tanaka, an additional contact would inherently have to be formed between the existing wiring layer and the additional wiring layer. Since the basic structure of the imaging device (e.g. Figure 6 of Nakashiba) teaches contacts having a longest length in the electric charge transfer direction, it would be obvious to use this contact shape when connecting the existing wiring layer to the additional wiring layer.

[claim 3]

Regarding claim 3, Nakashiba discloses a solid image pickup apparatus comprising: a pixel string in which a plurality of photoelectric converting sections corresponding to pixels are arranged in one string (Figure 6, Items 21); a CCD register, adjacently arranged to the pixel string, for successively transferring in a predetermined direction, signal charges photoelectrically converted in the respective photoelectric converting sections (Figure 6, Items 23); n (n is an integer of two or more) pieces of wiring layers formed in lamellar shape above the CCD register and its periphery (Figures 7A - 7D, Items 28a and 28c) via an insulating layer (Figures 7A - 7D, Item 25); and a contact having a longest length along an electric charge transfer direction (i.e. left to right along sheet 5 of the drawings, Figure 6) of the CCD register to at least one location between the

transfer electrode and the wiring layer (Figures 6 and 7A and 7C, contacts 27). However, Nakashiba does not disclose a contact between two wiring layers adjacent to each other via the insulating layer.

Tanaka et al. discloses a "double-layered transfer gate" structure (Column 5, Lines 11-25) which prevents the occurrence of pulse delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka with the transfer electrode of the Nakashiba to prevent the occurrence of pulse delay and rounding of pulse wave-forms when driving the solid state image pickup apparatus. When an additional wiring layer is added to the structure of the Nakashiba, as taught by Tanaka, an additional contact would inherently have to be formed between the existing wiring layer and the additional wiring layer. Since the basic structure of the imaging device (e.g. Figure 6 of Nakashiba) teaches contacts having a longest length in the electric charge transfer direction, it would be obvious to use this contact shape when connecting the existing wiring layer to the additional wiring layer.

[claims 5 and 6]

Regarding claims 5 and 6, Nakashiba discloses a wiring layer which is disposed to apply a voltage to at least one of the transfer electrodes of the CCD register (Figures 7A - 7D, Items 26a), an electrode other than the electrode of the CCD register (Figures 7A and 7C, lower horizontal section of items 28a and 28c); and a semiconductor area (i.e. the area below the wiring layers).

[claims 8 and 9]

Regarding claims 8 and 9, Nakashiba discloses a shift electrode which is formed between the pixel string and the CCD register and which transfers, to the CCD register, the signal charges photoelectrically converted in the respective photoelectric converting sections in the pixel string (Figures 6, 7B and 7D, Item 26b; c. 9, l. 66 - c. 10, l. 68); a shift electrode wiring layer for applying a voltage for transferring electric charge to the shift electrode (Figures 7A - 7D, Items 28b and 28d) and a contact which has a longest length along a direction crossing substantially at right angles to an electric charge transfer direction under said shift electrode and which connects the shift electrode to the shift electrode wiring layer (Figures 6, 7B and 7D, contacts 27).

[claims 10-12]

Regarding claims 10-12, Nakashiba lacks an upper-stage wiring layer formed above the shift electrode wiring layer and a contact which is formed in a strip shape along the electric charge transfer direction of the CCD register or along a direction crossing substantially at right angles to an electric charge transfer direction under the shift electrode and which connects the shift electrode wiring layer to the upper stage wiring layer.

Tanaka et al. discloses a "double-layered transfer gate" structure (Column 5, Lines 11-25) which prevents the occurrence of pulse delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka with the shift electrode of the Nakashiba to prevent the occurrence of pulse delay and rounding of pulse wave-

forms when driving the solid state image pickup apparatus. When an additional wiring layer is added to the structure of the Nakashiba, as taught by Tanaka, an additional contact would inherently have to be formed between the existing wiring layer and the additional wiring layer. Since the basic structure of the imaging device (e.g. Figure 6 of Nakashiba) teaches contacts having a longest length in the electric charge transfer direction, it would be obvious to use this contact shape when connecting the existing wiring layer to the additional wiring layer.

[claims 13-15]

Regarding claims 13-15, note that the Nakashiba in view of Tanaka lacks a n upper-stage wiring layer that is formed of a poly-silicon layer. Official Notice is taken that it is well known in the art to use doped poly-silicon as a wiring material for its ability to withstand higher operational temperatures (i.e. silicon has a higher melting point that commonly used metals such as aluminum). Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use poly-silicon as the material for the upper wiring layer to allow the device to operate at higher temperatures.

[claim 16]

Regarding claim 16, Nakashiba in view of Tanaka discloses a first wiring layer for applying a voltage for transferring electric charge to the transfer electrode of the CCD register (Figure 7A, Item 28a); a first contact which is formed into a strip shape along the electric charge transfer direction of the CCD register and which connects the transfer electrode to the first wiring layer (Figures 6 and 7A, Item 27); a shift electrode which is formed between the pixel

string and the CCD register and which transfers the signal charges photoelectrically converted in the photoelectric converting sections in the pixel string to the CCD register (Figure 7B, Item 26b; c. 9, l. 66 - c. 10, l. 68); a second wiring layer for applying the voltage for transferring electric charge to the shift electrode (Figure 7B, Item 28b); a second contact which is formed into a strip shape along a direction crossing at right angles to an electric charge transfer direction under the shift electrode and which connects the shift electrode to the wiring layer (Figures 6 and 7B, Item 27); a third wiring layer above the first wiring layer via the insulating layer (i.e. double-layered transfer gate taught by Tanaka, see claim 2 for further details); a third contact which is formed into a strip shape along the electric charge transfer direction of the CCD register and which connects the first wiring layer to the third wiring layer (a third contact would inherently be necessary, see claim 2 for further details); a fourth wiring layer formed above the second wiring layer via the insulating layer (i.e. double-layered transfer gate taught by Tanaka, see claim 11 for further details); a forth contact which is formed into the strip shape along a direction crossing at substantially right angles to an electric charge transfer direction under the shift electrode and which connects the second wiring layer to the fourth wiring layer (a fourth contact would inherently be necessary, see claim 11 for further details; and a shielding film formed above the third and fourth wiring layers via the insulating layer (Figure 7A - 7D, Item 28d).

[claims 17 and 18]

Regarding claims 17 and 18, note that the wiring layers (Figures 7A - 7D, Items 28a and 28c) do not over lap in a vertical direction (Figures 7A - 7D). The office notes that the additional gate structure of Tanaka would not change this feature as the additional gate wires only exist on top of the existing gate while the existing gates of the Nakashiba are spaced so that there is no overlap.

[claim 19]

Regarding claim 19, Nakashiba discloses a CCD register comprising a first transfer electrode (Figure 7A, Item 26a) to which a first voltage is applied, and a second transfer electrode (Figure 7B, Item 26b) to which a second voltage is applied, the voltage for transferring electric charge is applied to said first transfer electrode from a first wiring layer (Figure 6, Item Φ_1), the voltage for transferring electric charge is applied to said second transfer electrode from a fifth wiring layer (Figure 6, Item Φ_2), said first transfer electrode is connected to said first wiring layer via a first contact (Figures 6 and 7A, Item 27) formed into a strip shape along the electric charge transfer direction of said CCD register, and said second transfer electrode is connected to said fifth wiring layer via a plurality of contacts formed at predetermined intervals (Figures 6 and 7A, Item 27).

[claim 20]

Regarding claim 20, Nakashiba discloses a pixel string in which a plurality of photoelectric converting sections corresponding to pixels are arranged in one string (Figure 6, Items 21); a CCD register, adjacently arranged to said pixel string, for successively transferring, in a predetermined direction, signal charges photoelectrically converted in the respective photoelectric converting sections

(Figure 6, Items 23); a wiring layer (Figures 7A and 7C, Items 28a and 28c) formed above said CCD register and its periphery via an insulating layer (Figures 7A - 7D, Item 25), a shift electrode which is formed between said pixel string and said CCD register and which transfers, to said CCD register, the signal charges photoelectrically converted in the respective photoelectric converting sections in said pixel string (Figure 7B and 7D, Item 26b); a shift electrode wiring layer for applying a voltage for transferring electric charge to said shift electrode (Figure 7A and 7C, Items 28b and 28d); and a contact which is formed into a strip shape along a direction crossing substantially at right angles to electric charge transfer direction under said shift electrode and which connects said shift electrode to said shift electrode wiring layer (Figures 6, 7B and 7C, Item 27). However, Nakashiba does not disclose a wiring layer formed above a conductive layer via the insulating layer.

Tanaka et al. discloses a "double-layered transfer gate" structure including an upper-stage wiring layer (Figure 2, Item 36) formed above the electrode wiring layer or "conductive layer" via an insulating layer (Figure 2, Item 39; Column 5, Lines 11-25). The structure of Tanaka et al. prevents the occurrence of pulse delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka et al. with the wiring layers or "conductive layers" of the Nakashiba to prevent the occurrence of pulse delay and rounding of pulse wave-forms when driving the solid state image

pickup apparatus.

[claims 25 and 26]

Regarding claims 25 and 26, Nakashiba in view of Tanaka discloses all limitations except an electric discharge gate, disposed in parallel with said pixel string, for discharging the signal charge photoelectrically converted in said photoelectric converting section; a discharge wiring layer for applying an electric discharging voltage to said electric discharge gate; and a contact which is formed into a strip shape along a direction crossing substantially at right angles to an electric discharge direction in said electric discharge gate and which connects said electric discharge gate to said discharge wiring layer. Official Notice is taken that it is well known in the art to provide an electric charge discharge gate, wiring layer and contact as claimed to allow for the resetting of pixel photodiodes prior to the start of integration to have a consistent base level charge for each picture. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a discharge gate, wire and contact as claimed to allow for resetting the array.

[claim 27]

Regarding claim 27, Nakashiba discloses a solid image pickup apparatus comprising: a pixel string in which a plurality of photoelectric converting sections corresponding to pixels are arranged in one string (Figure 6, Items 21); a CCD register, adjacently arranged to the pixel string, for successively transferring, in a predetermined direction, signal charges photoelectrically converted in the respect photoelectric converting sections (Figure 6, Items 23); a wiring layer (Figures 7A

and 7C, Items 28a and 28c) formed above the CCD register and its periphery via an insulating layer (Figures 7A - 7D, Item 25); a first contact having a longest length along an electric charge transfer direction of the CCD register and connected to the wiring layer (Figures 6, 7A and 7C; Item 27); a shift electrode, formed between said pixel string and the CCD register, for transferring the signal charges photoelectrically in the photoelectric converting sections in the pixel string to the CCD register (Figures 7B and 7D, Item 26b; c. 9, l. 66 - c. 10, l. 68); a first wiring layer for applying the voltage for transferring electric charge to the shift electrode (Figures 7B and 7D, Items 28b and 28d). However, Nakashiba lacks a second wiring layer formed above said first wiring layer via the insulating layer; and a contact which is formed into a strip shape along the electric charge transfer direction of said CCD register and which connects said first wiring layer to said second wiring layer.

Tanaka et al. discloses a "double-layered transfer gate" structure including an upper-stage wiring layer (Figure 2, Item 36) formed above the electrode wiring layer via an insulating layer (Figure 2, Item 39; Column 5, Lines 11-25). The structure of Tanaka et al. prevents the occurrence of pulse delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka with the shift electrode of the Nakashiba to prevent the occurrence of pulse delay and rounding of pulse wave-forms when driving the solid state image pickup apparatus. When an additional wiring layer is added to the structure of the Nakashiba, as taught by Tanaka, an

additional contact would inherently have to be formed between the existing wiring layer and the additional wiring layer. Since the basic structure of the imaging device (e.g. Figure 6 of Nakashiba) teaches strip shape contacts formed in the electric charge transfer direction, it would be obvious to use this contact shape when connecting the existing wiring layer to the additional wiring layer.

[claims 28 and 29]

Regarding claims 28 and 29, Nakashiba discloses a shift electrode, formed between said pixel string and the CCD register, for transferring the signal charges photoelectrically in the photoelectric converting sections in the pixel string to the CCD register (Figures 7B and 7D, Item 26b; c. 9, l. 66 - c. 10, l. 68); a first wiring layer for applying the voltage for transferring electric charge to the shift electrode (Figures 7B and 7D, Items 28b and 28d). However, Nakashiba lacks a second wiring layer formed above the shift electrode wiring layer and a contact which is formed in a strip shape along the electric charge transfer direction of the CCD register which connects the first wiring layer to the second wiring layer.

Tanaka et al. discloses a "double-layered transfer gate" structure (Column 5, Lines 11-25) which prevents the occurrence of pulse delay and rounding of pulse wave-forms (Column 1, Lines 44-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the double-layered transfer gate structure of Tanaka with the shift electrode of the Nakashiba to prevent the occurrence of pulse delay and rounding of pulse wave-forms when driving the solid state image pickup apparatus. When an additional

wiring layer is added to the structure of the Nakashiba, as taught by Tanaka, an additional contact would inherently have to be formed between the existing wiring layer and the additional wiring layer. Since the basic structure of the imaging device (e.g. Figure 6 of Nakashiba) teaches contacts having a longest length in the electric charge transfer direction, it would be obvious to use this contact shape when connecting the existing wiring layer to the additional wiring layer.

7. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Nakashiba (US 5,442,396) in view of Tanaka et al. (US 5,506,429) as applied to claims 2 and 3 above, and further in view of Wakayama et al. (US 5,736,756).

[claims 22 and 23]

In regard to claims 22 and 23, note that the Nakashiba in view of Tanaka et al. discloses all limitations except for a diffusion area formed adjacent to said CCD register; a substrate wiring layer for applying a predetermined voltage to a substrate through said diffusion area; and a contact which is formed into a strip shape along the electric charge transfer direction of said CCD register and which connects said diffusion area to said substrate wiring layer.

Wakayama et al. discloses a solid-state image sensing device with a light shielding film (Figure 1, Item 24) which contacts a diffusion area on the substrate (Figure 1) , and a potential applying means (Figure 1, Item 26) which reduces smear and dark current in the image sensor (Column 2, Lines 55-60). The office notes that the light shielding film comprises a contact (i.e. the sections running

perpendicular to the substrate) and a wiring layer (i.e. the sections running parallel to the substrate). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a light shielding film such as that of Wakayama et al. to reduce smear and dark current in the imager of the Nakashiba in view of Tanaka et al.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J. Henn whose telephone number is (571) 272-7310. The examiner can normally be reached on M-F 9:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber can be reached on (571) 272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).